# FPGA-Based Single Wire Aggregation (SWA) for FPGA and Non-FPGA Designers

**A Lattice Semiconductor White Paper.**

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When it comes to electronic systems, the connectors used to link circuit boards and modules are costly, they consume valuable real estate on the board and space in the system, and they degrade the reliability of the product.

Lattice has developed an innovative new way for system architects and developers to use tiny, low-cost FPGAs to dramatically reduce the number of board-to-board xd and module-to-module connectors, thereby increasing the reliability of the system while also reducing its size and cost.

This solution can be customized by developers with FPGA design experience. Even better, it can be quickly and easily deployed by developers with no FPGA experience whatsoever.

## Making Good (or Bad) Connections

The vast majority of today's electronic systems involve two or more circuit boards and/or modules. (For the remainder of this paper, unless otherwise stated, the term "circuit boards" or "boards" will be assumed to encompass "modules.")

A perennial problem for system designers is connecting the boards together in order to transfer data between them. A very common solution is to mount multi-pin connectors on the boards and to use multi-wire harnesses or flex to link the boards together.

Unfortunately, each connector pin is a potential point of failure, so in addition to adding cost and consuming space, connectors are often the overwhelming factor regarding the reliability -- or lack thereof -- in an electronic system. This means that minimizing the number of inter-board connections reduces cost, reduces space, and increases the reliability of the system.

As illustrated in Figure 1, many of these inter-board signals typically provide only relatively low speed communications using general-purpose input/outputs (GPIOs) or serial interfaces like $I^2C$ (inter-integrated circuit) and $I^2S$ (integrated inter-IC sound bus).

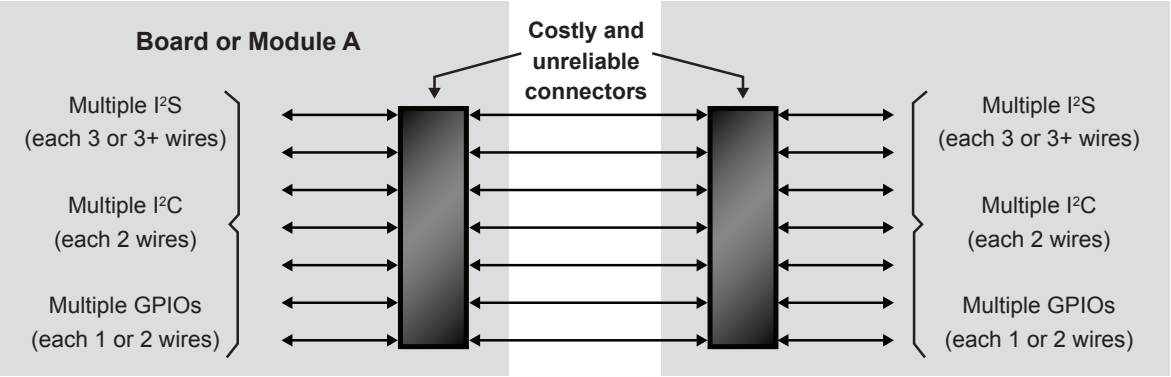


***Figure 1: Traditional connectors are costly, consume space, and degrade the reliability of the system.***

Designers of a wide range of systems -- from handhelds to notepad computers to industrial controllers -- desperately want to minimize the number of connector pins and inter-board wires.

## Single Wire Aggregation: The FPGA Advantage

The idea behind single wire aggregation (SWA) is to take multiple signals and aggregate them into a time division multiplexed (TDM) signal that requires only a single inter-board wire. One way to do this would be to create a custom application-specific integrated circuit (ASIC) for each product (Figure 2).

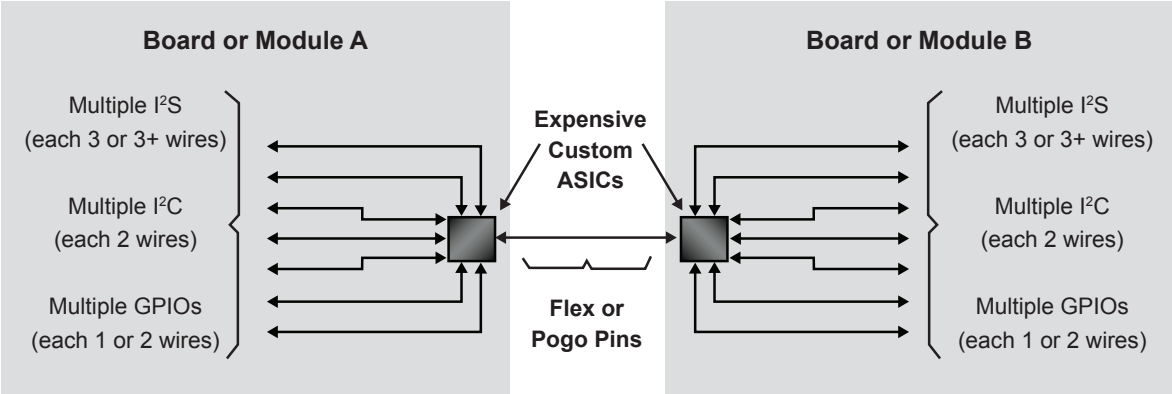


***Figure 2: Custom ASICs are expensive, time-consuming to develop, and inflexible.***

Unfortunately, there are multiple disadvantages associated with custom ASIC solutions, including the fact that they are expensive and time-consuming to develop. Even worse, any algorithms and functions they contain are effectively "frozen in silicon," which means they cannot adapt to changing requirements, such as the head of sales unexpectedly announcing: "Our biggest customer says we need to replace one of the I²S interfaces with two I²C channels."

The solution is to use low-cost field-programmable gate arrays (FPGAs), such as iCE40 UltraPlus™ devices from Lattice Semiconductor (Figure 3).

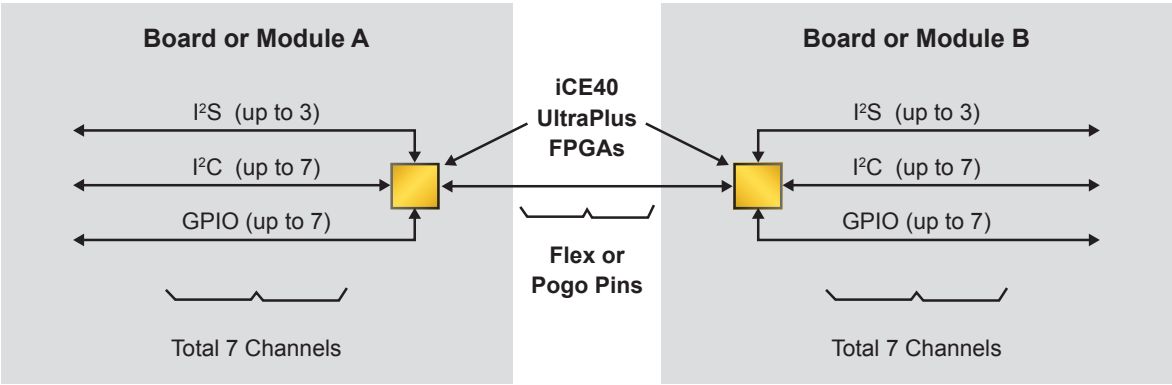


***Figure 3: FPGAs are inexpensive and extremely flexibl e.***

One huge advantage of using FPGAs to implement single wire aggregation is that they are extremely flexible and can be quickly and easily customized to implement the required numbers and types of the various communications channels.

## iCE40 UltraPlus-Based SWA for FPGA Designers

The statement in the preceding paragraph -- that “FPGA-based SWA solutions can be quickly and easily customized” -- comes with a small caveat, which is that you have to be familiar with designing FPGAs.

If you are an FPGA designer, then Lattice provides some of the easiest-to-use FPGA development tools in the industry. Furthermore, in the case of its SWA solution, Lattice provides full reference design resources for use with its industry-leading iCE40 UltraPlus™ FPGAs:

- The source code for an easily modifiable parameterized SWA reference design ready to run on the Lattice Radiant design tool.
- Free access to the Lattice Radiant® design tool.
- An associated Reference Design User Guide.
- An SWA demonstration and development board.

Unfortunately, not every design team has access to FPGA design expertise. Fortunately, Lattice also has solutions for non-FPGA designers.

## iCE40 UltraPlus-Based SWA for Non-FPGA Designers

Consider a system based on a microcontroller (MCU). Some members of the design team will be skilled in developing software using a language like C or C++, and then running a software compiler, which takes the program and generated an executable file in machine code. Other members of the team can load this machine code file into the MCU without being required to know anything about writing programs.

Similarly, FPGA developers have expertise in capturing designs using hardware description languages (HDLs) like Verilog or VHDL, and then running a hardware compiler called a logic synthesis engine, which takes the HDL and generates a configuration file, also known as a bitstream. Other members of the team can then load this bitstream into the FPGA without having to know anything about designing FPGAs.

The first SWA solution for non-FPGA designers is based on Lattice providing a suite of five pre-synthesized bitstreams (Figure 4). These configurations, which are based on an analysis of multiple real-world products, have been selected to address the requirements of a wide range of system designs.

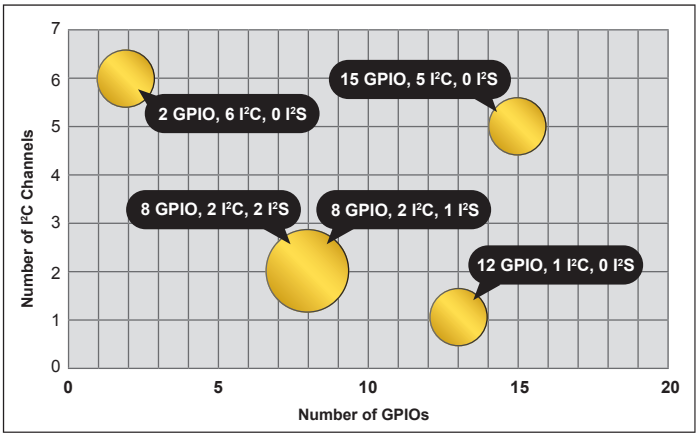


***Figure 4: Pre-compiled bitstreams are available for five popular configurations.***

A Bitstream User Guide is available from Lattice's SWA webpage (latticesemi.com/singlewire). This guide describes how anyone can load one of the preconfigured bitstreams into an iCE40 UltraPlus FPGA.

But wait, there's more, because Lattice also offers a free SWA design service. If you visit Lattice's SWA development board webpage (latticesemi.com/products/developmentboardsandkits/singlewire), you can use an interactive form to specify the unique combination of channels you require for your design, and the Lattice design team will email the corresponding bitstream file to you.

## iCE40 UltraPlus FPGAs

For the purposes of this paper, it's necessary to provide only a high-level overview of these devices. iCE40 UltraPlus FPGAs boast a flexible logic architecture with 2800 or 5280 4-input look-up tables (LUTs), customizable general-purpose input/output (GPIO), up to 80 kilobits of embedded block memory (EBM), and up to 1 megabit of embedded SRAM.

In addition to featuring an ultra-low-power advanced process with static current as low as 75 uA and as little as 1 to 10 mA active current for most applications, iCE40 UltraPlus FPGAs are also available in multiple package options to fit wide range of applications needs, from an ultra-small 2.15 x 2.50 mm WLCSP package optimized for consumer and IoT devices to a 0.5 mm pitch 7 x 7 mm QFN for cost-optimized applications.

Of particular interest is the fact that the configuration bitstream can be loaded directly into SRAM-based configuration cells, thereby allowing iCE40 UltraPlus FPGAs to be reprogrammed over and over again. This is the best option during the prototyping phase of a project, because it allows you to experiment with different designs and bitstreams.

If the SRAM-based configuration approach is used when the iCE40 UltraPlus is deployed in a product, then the configuration can be loaded via an on-board MCU or from an external SPI Flash memory device.

Alternatively, iCE40 UltraPlus FPGAs also contain a one-time programmable (OTP) on-chip non-volatile configuration memory (NVCM), which is best suited for mass production. Once the NVCM has been programmed, the device will automatically, quickly, and securely boot from this configuration.

## The SWA Demonstration and Development Board

The SWA demonstration and development board contains two iCE40 UltraPlus FPGAs. One is used as a data generator or data verifier, the other is used to implement a SWA reference design (either a Controller or a Peripheral).

A typical scenario will involve two of these boards as illustrated in Figure 5. In this example, the board on the left contains the Data Generator and the SWA Controller, while the board on the right contains the SWA Peripheral and the Data Verifier.

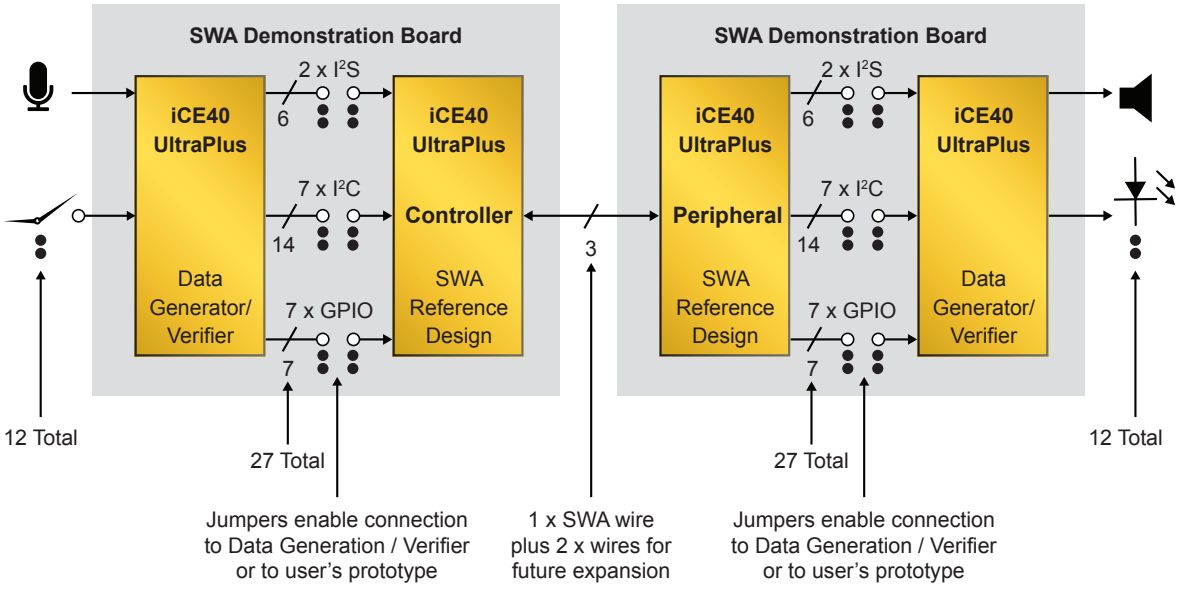


***Figure 5: Block diagram of example SWA demonstration board setup.***

Observe the jumpers. If these are left in place, the data from the data generator on the demonstration board on the left will be fed into the SWA Controller reference design, which will aggregate it into a single signal for transmission to the board on the right. In turn, the SWA Peripheral reference design on the right-hand demonstration board will receive the aggregated signal and feed the de-aggregated components to the data verifier. This use-case is also reflected in Figure 6(a).

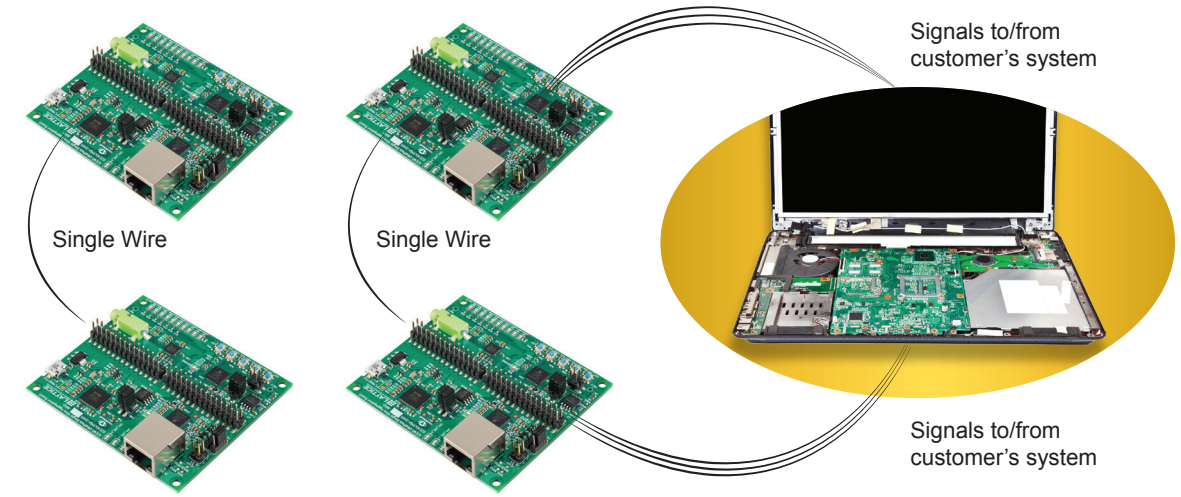


***Figure 6. Two example use cases.***

## Bits and Bytes

As noted above, the SWA reference design runs on two iCE40 UltraPlus FPGAs to aggregate multiple data streams such as I²C, I²S, and GPIO in TDM fashion by one FPGA and send it over a single wire to the other FPGA for de-aggregation back to the same set of streams.

The single wire communication between the FPGAs runs around 7.5 megabits-per-second (Mbps). The design is also configurable -- the number of I²C/I²S busses and GPIOs and single wire protocol packet length can be adjusted, and the single wire protocol between the FPGAs is robust with error detection and retry features. A brief summary of the various features is as follows:

- Up to seven channels can be aggregated.
- The raw data rate on the single wire interface is ~7.5 Mbps or higher.
- The system supports variable packet length for efficient use of the single wire bandwidth.
- A retransmit feature is offered when a parity error is detected on the receiver side.
- The system supports both I²C Fast-mode (400 kbps) and Fast-mode Plus (1 Mbps).
- I²C Interrupts can be realized using GPIO with event-based transmission.
- I²S supports single stereo channel, 48K Hz sampling rate, with up to 32 bits per sample, and with bi-directional support.

## Summary

Many of today's electronic systems involve multiple circuit boards. Furthermore, many of these systems use multiple interfaces of different types -- like I²C, I²S, and GPIO -- to collect data from peripherals and sensors and to communicate this data between boards.

In addition to the fact that routing signals through congested boards and connectors can present its own challenges, circuit board real estate is often at a premium, as is the space within the system's enclosure. In addition to increasing cost and taking up space, connectors are often the most unreliable components in the system.

Lattice has developed an innovative new way for system architects and developers to use tiny, low-cost FPGAs to implement single wire aggregation, which can dramatically reduce the number of inter-board connections, thereby increasing the reliability of the system while also reducing its size and cost.

This solution can be customized by developers with FPGA design experience. Even better, it can be quickly and easily deployed by developers with no FPGA experience whatsoever.