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Designing High Performance Interposers with 3-port and 6-port S-parameters

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Abstract

The use of interposers is important for debug, signal measurement and validation of interconnects in memory systems. As speed increases, the effect of the interposer on signal integrity of the system grows, and cannot be ignored. It is important to understand the performance of the system after the interposer is added. Scattering parameters are a good way to capture the performance of the interposer. The S-parameter data can be used to interpret the performance characteristics, in system level simulation to evaluate jitter and eye opening, and to create de-embedding filters for oscilloscopes, essentially removing the influence of the interposer from the scope waveform.

This paper will interpret multiport S-parameters for several memory interposer design cases. This will help the audience understand some of the performance characteristics that can be inferred from the S-parameters, as well as some of the interactions between the interposer and the device under test and probing system. From a system level design perspective, reviewing this data helps the engineer to have confidence in probing implementation, whether the engineer is designing or using a purchased interposer. This paper follows a DDR4 design case that will be carried forward to be used with de-embedding information for a post-production oscilloscope measurement. Finally, VNA measured S-parameters of the fabricated interposer will be compared to the extracted pre-production S-parameters thus validating the S-parameter extraction process.

This paper will progress through suggestions of how to relate frequency domain performance to physical design, physical characteristics versus edge rate, insertion and return loss values and interaction, linearity, the effects of probe and system noise, and through path performance effects on the complete system.

The design and use of memory measurement interposers has to be carefully thought out to avoid performance degradation of the system under test, while at the same time providing accurate and repeatable measurements. This paper adds to existing interposer literature by offering a state of the art perspective for the design and use of an interposer for probing DDR4 memory packaging at speeds that are difficult to achieve. The effects of the physical structure of the interposer can't be ignored, so the careful designed of the interposer is needed to yield valid measurement results. This paper explores the challenges and solutions to successful interposer design.

Author(s) Biography

Joseph Socha is a Senior Signal Integrity Engineer at Nexus Technology. His past experiences are many: Joe managed the Signal Integrity group for Sedona International and Plexus. He has presented talks at several IBIS summits, IPC and PCB West. He has designed equipment for computer systems, robotics, oceanography, and control systems. Over the last 20 years, Joe has specialized in signal integrity, timing analysis, and high-speed design. During this time, he gained expertise in EDA methodologies for high-speed design, IBIS models, and circuit and topology simulation. As a consultant, his expertise has been sought by a variety of small and large companies. Joe graduated from Merrimack College, Massachusetts, with a bachelor's degree in electrical engineering.

Jonathan Dandy is a Senior Hardware Engineer in the Probes group at Tektronix. Presently he is working on signal integrity solutions for high-frequency probing applications. Jonathan has 13 years of experience in analog design working on current, high-voltage and high speed probes as well as medical electronics. Jonathan graduated with a Master's Degree in Electrical Engineering from Kansas State University.

Philip Pun is a Principal Design Engineer at Cadence Design Systems responsible for SoC, package and board signal & power integrity for DDR PHY. Previously he was involved with the design of high performance Network Processors and Catalysts 2/3/4K gigabit switches at Cisco Systems. He received his M.S., degree in Electrical Engineering and B.S.BMEE., degree from the Univ. of Southern California.

Prashanth Thota is the Memory Solutions Product Planner and Product Marketing Manager at Tektronix. He has over 14 years of experience at Tektronix and has held various positions in the engineering roles designing Logic Analyzer products, prior to the current role. Prashanth graduated with an Engineering degree in Electronics and Communication from University of Mysore followed by an Executive Management Degree from Indian Institute of Management Calcutta.

Background

Today's electronic systems are often designed with fine pitch devices below a millimeter and operate at speeds above a Gigahertz. Printed circuit boards (PCB) are densely packed to accommodate signal routings, System on Chip (SoC) devices and passive components. In mobile products, some may require dual side mounting and advanced stackable packaging technology such as Package on Package (PoP). This can make it nearly impossible to access or measure these signals. Considering that many of the signals of interest are high-speed, probing "close" to signal pin may not be close enough to prevent anomalous readings on the measurement equipment. One way to improve access to these signals is to place an interposer between the main PCB and the target device of interest to improve access to the device pins.

Figure 1- Interposer Example with Probes attached

Anatomy of an interposer

An interposer is a small circuit board that is inserted between the device to be probed and the target system. This board allows the signal to be broken-out for probing with an instrument like an oscilloscope, logic or protocol analyzer. This "breakout board" method has been around since the 1980's. What is different now is that this method needs to work at multi-Gigabit speeds. In recent years these breakout boards have gotten smaller and faster and are generally known as Interposers. An example is shown in Figure 1. Basic SPICE equivalent models are sometimes available for simulations to help quantify the interposer induced disturbances and circuit interaction. In this paper we will be taking modeling to the next level using S-parameters and explore the technical challenges behind the high-performance interposers. Using this method of modeling allows us multiple uses of the S-parameter model. It can be used for the design of the interposer, to de-embed the interposer from hardware measurements and correlate the extracted S-parameters with Vector Network Analyzer (VNA) measurements of the interposer.

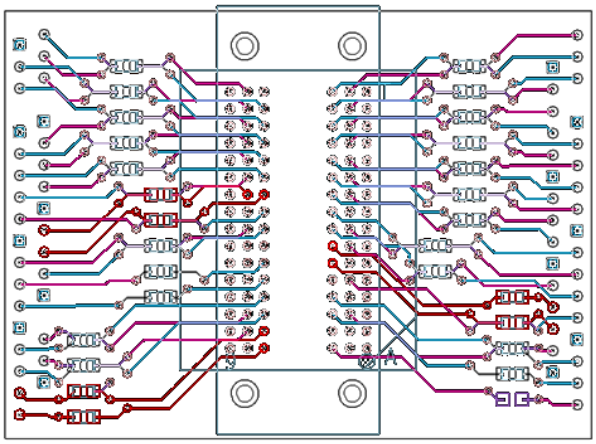

Figure 2 - A Memory Breakout board layout

For illustration purposes the physical description and many of the performance graphs will be based on the memory breakout board layout in Figure 2. This breakout board is a low performance design and yields easily identifiable results in the S-parameter plots which were extracted using the PowerSI tools.[1] The graphs-parameter plots will be compared and contrasted with a DDR4 interposer used later in the simulation and measurement sections of the paper.

Interposers can utilize power and ground planes, buried resistors, specialized PCB materials, and specialized pads or connectors for probe attachment. From Figures 1 and 3 you can clearly see how the interposer is placed in-between the device of interest and the rest of the system. The PCB layout view in Figure 2 shows how the thru connection (top to bottom) also has a trace connecting the signals to a location convenient for physical measurement. Figure 3 shows a cross-section view of the system. Most engineers will recognize that a break out trace would appear as a stub to the system. In order to minimize the stub effect between the component pin and the probe point, a series dampening resistor is used, and is referred to as the Tap resistor.

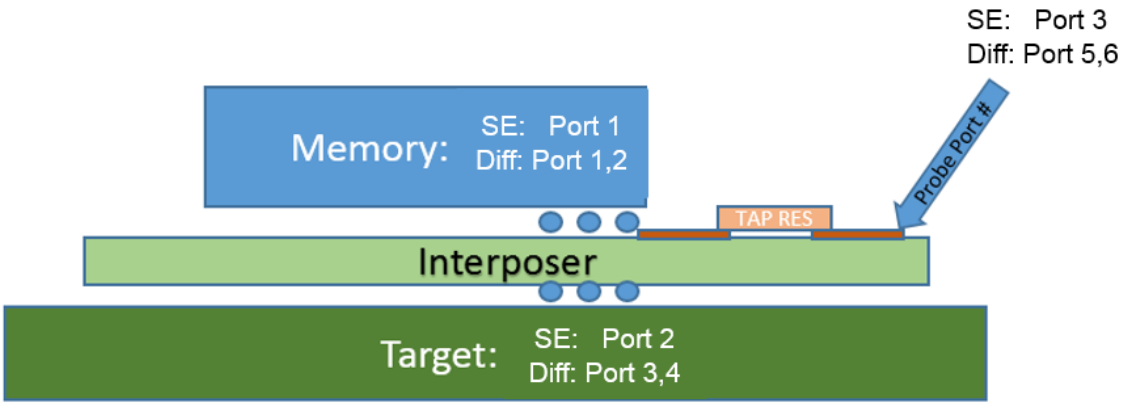

Figure 3 - Cross section block diagram of interposer

[1] Cadence Sigrity PowerSI – from Cadence Design Systems

Interposer Ports and Signal Flow

Figure 3 above is basically an electrical network that can be described as a 3-Port network. We assigned a port at each connection for the memory device, the target system and the probe. For convention we will locate Port 1 at the memory device and Port 2 at the target and Port 3 as the probe point. Signal transmission between ports follows the n-port theory convention beginning with the output port number followed by the input port. For example, S_{21} represents signal transmission from Port 1 to Port 2 and S_{31} for signal from Port 1 to Port3.

For differential signals the number of ports would double and you would have a 6 port S-parameter description of interposer. The S-parameters would capture not only the intended signal paths but also the coupling between. For convention ports 1 and 2 are at the memory device, ports 3 and 4 are at the target and ports 5 and 6 at the probe. The odd numbered ports make up the True side of the differential pair and the even numbered ports the Complement side of the pair.

Interposer Use Cases

The classic modeling effort would involve measuring the interposer with a Vector Network Analyzer (VNA). During the measurement each port is terminated by 50 ohms. This process and findings is described in the Interposer Characterization section of the paper. While this is a necessary model for de-embedding and correlation, the 50 ohm loading at all ports may mask some of the important performance characteristics that are needed in the design process. Using additional models with both loaded and unloaded conditions can lend some further insight to a high-performance interposer design.

The example in Figure 3 has many of the signals routed out to probe points. In most cases users are only able to probe a few signals at a time. This leads to two use cases that need to be modeled. First consider the un-loaded case where there is no external probe attached to the probe point. In this case energy flows from Port 1 to both Port 2 and Port 3. Consider that Port 3 is not connected; the energy that flows from Port 1 to Port 3 should be reflected back at this high impedance discontinuity. This effect will show up in the return loss (S_{11}) of the model. There are many factors in the interposer design that affect S_{11}; the most significant is the distance from the through connection to the tap resistor. For the purposes of illustration the PCB design in Figure 2 was given no special consideration for this trace in order to clearly make this effect observable.

The second use case is where the probe is attached at the probe point at Port 3. This use case is complex because most oscilloscope probes have a frequency dependent behavior. As in the un-probed case there is some of the energy that flows from Port 1 to Port 3 and in this use case some of the energy will be dissipated at port 3 by the probe. The amount of energy dissipated varies as the frequency varies. Typically probes will have higher impedance at lower frequencies and lower impedance at higher frequencies. More details are described in the measurement section of the paper. Given that a scope probe at Port 3 has some frequency dependent losses, the S_{21} and S_{11} profiles for the unloaded case and the probed case will be different. This is shown in Figure 4 below.

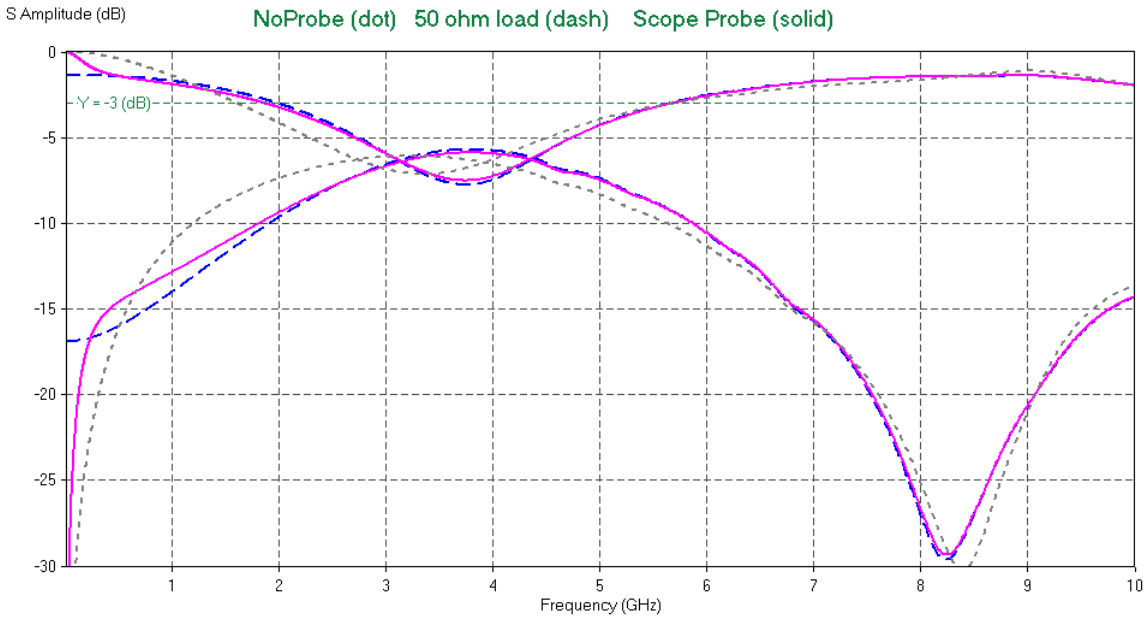

Figure 4 – Breakout Board Loading Condition Overlay

Interposer Design Challenges

A key design goal for the interposer is to have good transmission from Ports 1 to 2 while isolating the loading effects from Port 3. This is the first challenge. Factors such as trace width, dielectric material and distance to the tap resistor have significant impact on interposer S-parameters. Other factors such as copper surface roughness and glass weave density have a more subtle impact at the frequencies of interest. While there are numerous other variables that can impact the overall performance, it would not be practical to simulate all possible combinations in a reasonable amount of time. Spending simulation time to optimize critical parameters can yield a practical interposer design solution with very good performance.

The second challenge is making each signal have uniform insertion loss, return loss, isolation and delay. There are manufacturing limitations on what can be built with the current PCB fabrication as well as time and cost restrictions on making every topology the same throughout the design. These limitations will affect the S-parameters. Once the interposer is designed and ready to be built, it is time to compare all the 3-port S-parameters and 6 port S-parameters on the interposer as a group. With an ideal layout implementation case each signal would look exactly the same. If you looked at all of them at the same time they would appear as one line. This implies that deviation in the individual S-parameter waveforms is related to the differences in implementation of each topology.

For clarity we will continue with the breakout board layout example from Figure 2 to show an overlay of all the signals in this example layout which have varying topologies.

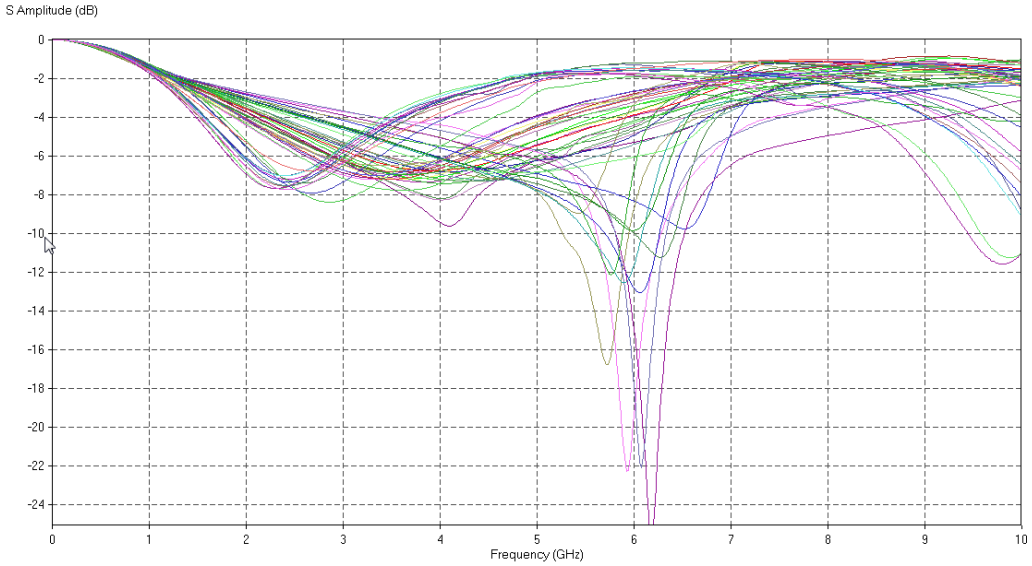

Figure 5 - Breakout board Insertion Loss overlay

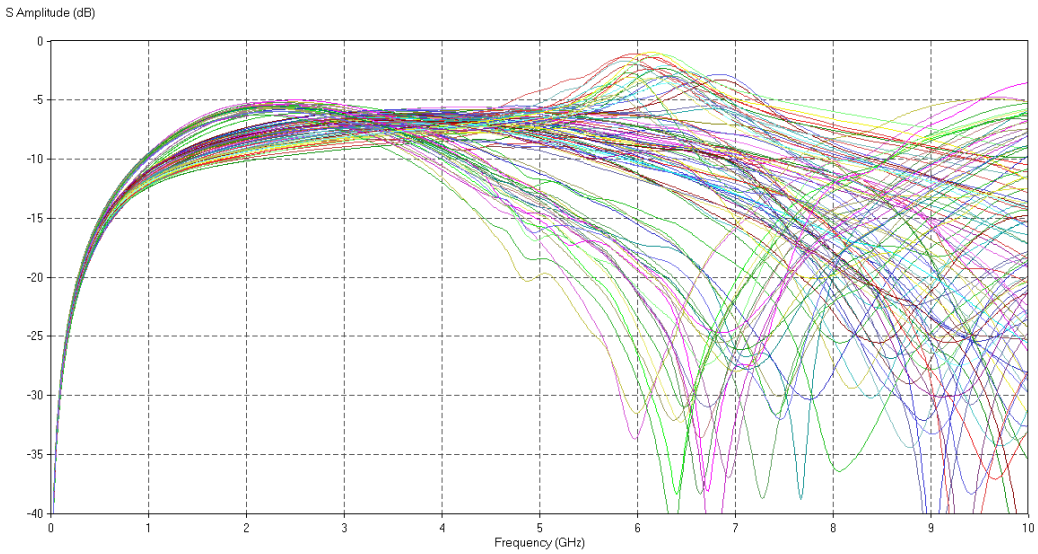

Figure 6 - Breakout board Return Loss overlay

Clearly this break out board design has a lot of variations in the topology and hence a lot of variations in the S-parameters. You will observe 3 major groupings of waveforms: looking at the insertion loss graph look for sub groups of similar shapes at 2.5 GHz, 4 GHz, and 6GHz. The return loss graph shows three sub-groupings as well, suggesting that the layout has three topology groups.

Key metrics in the S-parameters

Insertion loss from port 1 to port 2 is an important metric. Commonly the -3dB point is used to compare interposer performance. Below are two graphs, Figure 7 is the unloaded or no-probe case and Figure 8 is the probed case where a scope probe model is attached to Port 3. The thicker lines in the graph are insertion loss and the thinner lines are return loss. Pink lines are the breakout board and Blue is the DDR4 interposer.

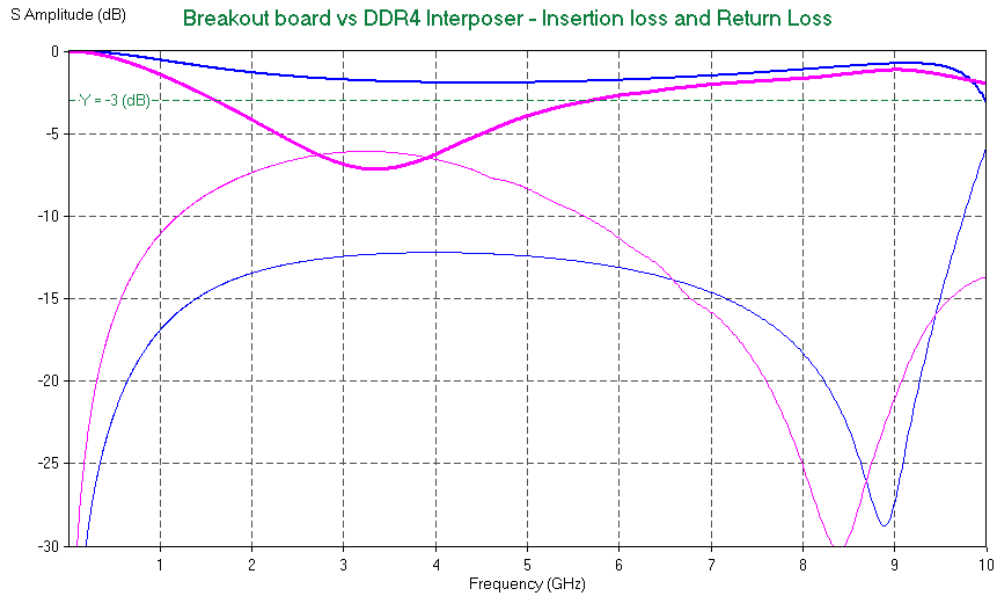

Figure 7- Breakout board and DDR4 interposer single bit Insertion and Return loss graph in the unloaded use case

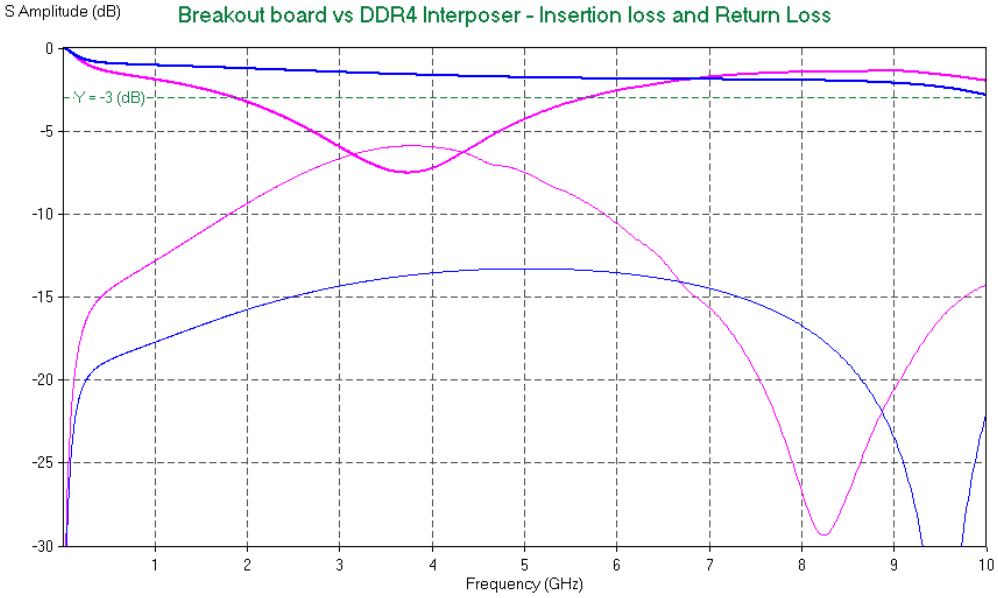

Figure 8 - Breakout board and DDR4 interposer single bit Insertion and Return loss graph in the Probed use case

Note that the bandwidth in the breakout board for is about 2.5GHz and the DDR4 interposer is 10GHz. Return loss at -10dB is another key metric. For the frequency range of interest, reflected energy below this -10dB mark will not significantly change the driver waveform.[2] Note that the -10dB point for return loss in the Breakout board for is about 1.25GHz and the DDR4 interposer does not go above -13dB.

As a general guideline, the measurement system should be 3 to 5 times faster than the highest signal to be measured.[3] The breakout board's 1.25GHz bandwidth corresponds to

[2] Eric Bogatin - How much return loss is too much?: Rule of thumb #12 May 21, 2014
[3] http://www.tek.com/document/technical-brief/tekconnect-probes-signal-fidelity-issues-and-modeling

a system with a 1.4ns risetime such as a 500MTS (250MHz clock) bus. The DDR4 interposer will be five times faster than a 175ps edge typical of a 4000MTS (2GHz clock) bus. The performance of each of these examples could be dramatically improved if the interposer is de-embedded from the system as discussed in the De-embedding a DDR4 Interposer and Probe section.

DDR4 Simulation and System Measurement

The DDR4 memory sub-system used for simulation and lab measurement correlation is a test validation platform implemented with a SoC DDR controller chip and two DDR4 unbuffered DIMMs. Between the memory controller and the DDR4 memory I/O's is the DDR channel that includes the SoC package, PCB, connector, DIMM card, DDR4 interposer and the memory package. Typical FR4 material and technology are used in the construction of the test board and DIMM. Figure 9 shows the dual DIMM arrangement on the test board and Figure 10 depict the corresponding cross sectional interconnect view.

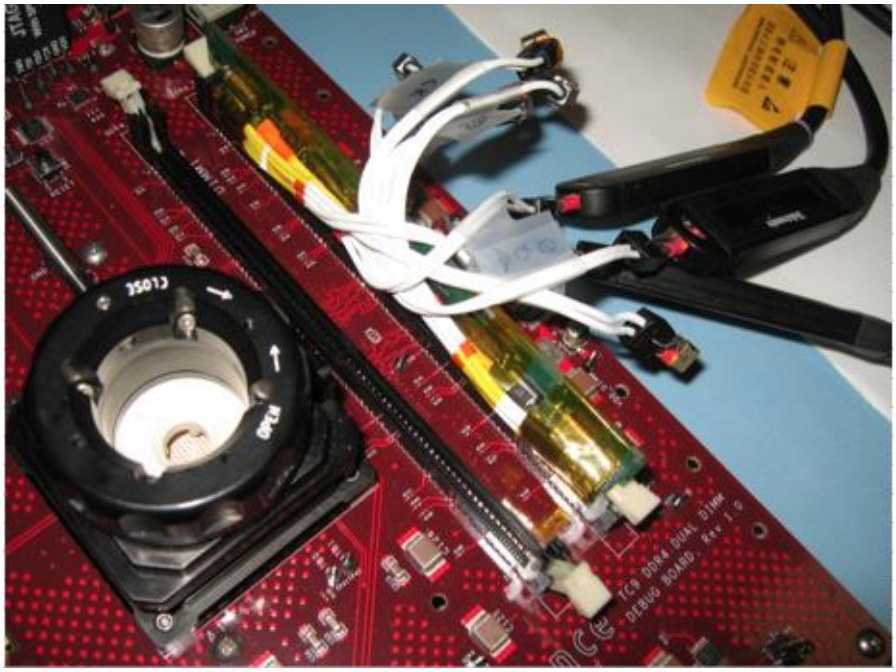

Figure 9 - DDR4 memory system validation platform and lab setup

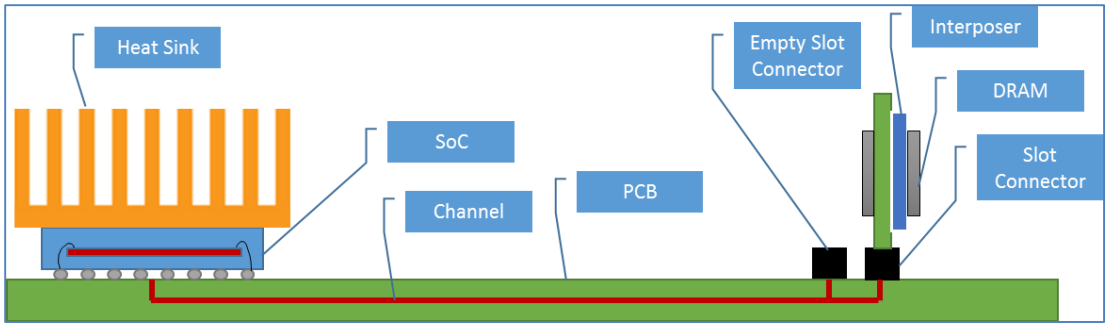

Figure 10- Cross section of DDR4 memory sub-system interconnects

Accurate modeling and simulations are essential in the design of high-speed DDR4 memory interfaces; otherwise critical design goals cannot be met. For example, during the design and implementation of the chip, package and board interconnects, simulation results are necessary to optimize the output drive performance, trace impedance, ODT terminations, PCB routing constraints and delay matching among the data bits. The ability to detect potential performance problems can help reduce the high cost of silicon and system prototype respins. System-level simulation greatly increases the chance of success. Figure 11 shows the interconnect circuit topology along the signal path between the SoC and memory.

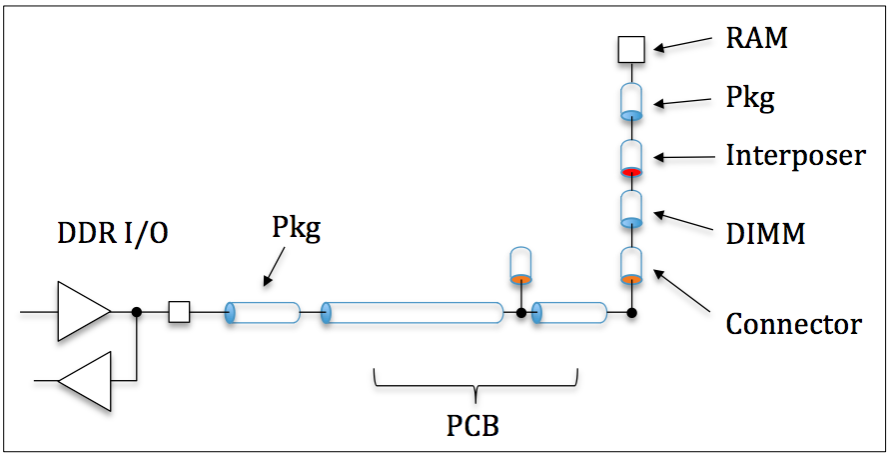

Figure 11- DDR4 Memory Channel Topology

The traditional modeling approach uses RLGC elements to construct models for the electrical interconnects. But, if insufficient numbers of T- or Pi- elements are used, the frequency response would be limited. To increase the bandwidth of the models, S-parameter modeling is used for design extractions and VNA measurements to capture the broadband characteristics. For DDR4 at 2400 data rate, the signal rise and fall times are on the order of 200ps to 300ps and the primary energy content of the signal is below the 5^{th} harmonic of the fundamental frequency. The magnitude of the energy content is approximately -60dB at 6GHz. So we can capture fairly good electrical characteristics at least to 6GHz without significant compromise in the fidelity of the interconnect models.

Fig 12 shows the simulated FFT spectrum of the signal content in the DDR4 channel at the RAM input.

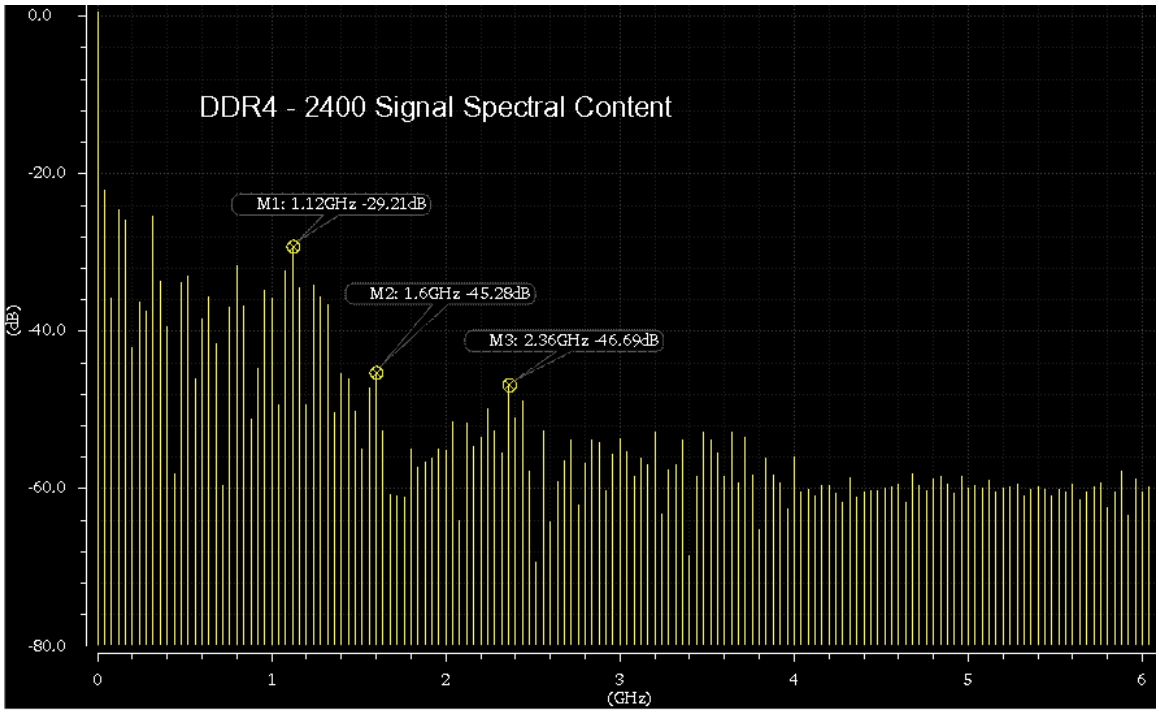

Figure 12- FFT Spectrum of DDR4 Waveforms

Time domain simulations with the use of SPICE simulators remain the industry's standard for analyzing linear and non-linear circuits. With the increased use of S-parameter models, one of the key challenges is numeric convergence. The latest SPICE software and algorithms are capable of handling S-parameter models in complex circuit topologies. Simulations of the DDR4 I/O's using IBIS I/O models and S-parameter interconnect models were done using the APS Spectre SPICE simulator. Lab measurements of actual hardware setup with the DDR interposer provide correlations to help validate the modeling, analysis and measurement techniques presented in this effort. Figure 13 shows the simulation waveforms.

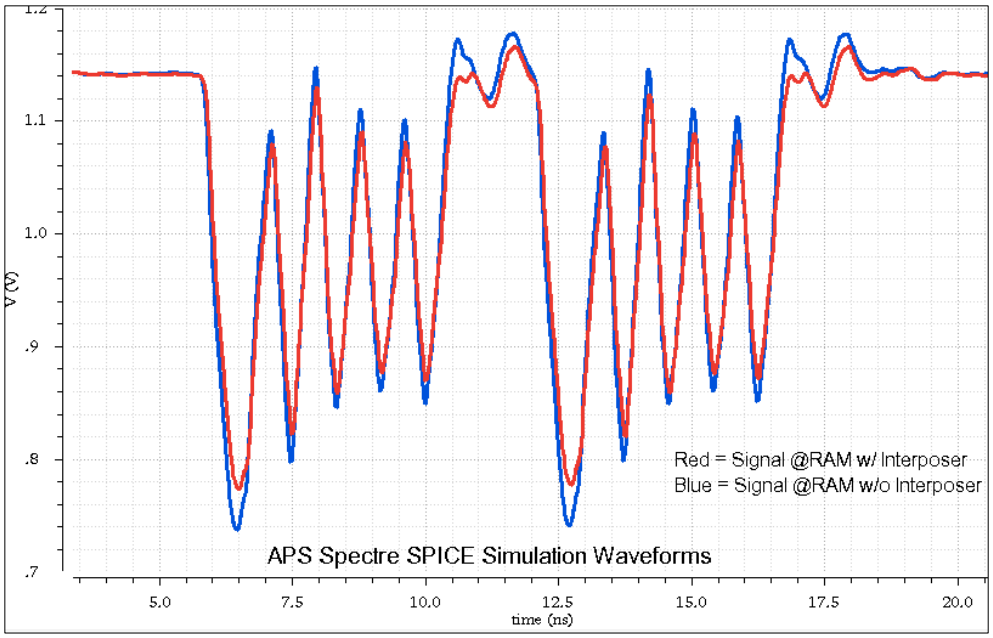

Figure 13- DDR4 Memory Time-Domain Channel Simulation

A key point of interest is whether the DDR interposer provides an effective method of probing with minimal electrical impact to the signal path. Comparison between the simulated waveform with and without the DDR interposer shows that the interposer has minimal loading impact on the signal.

Figure 14- DDR4 Memory Lab Measurements with DDR4 Interposer

Lab measurements with an oscilloscope connected using an interposer also correlated well with the simulation results. Figure 14 shows the waveforms for DQS0 and Strobe signals captured on the scope. The signal amplitude, stub reflections and ISI are observed both in simulation and measurement.

For high data rate analysis above DDR2400, the industry is moving toward frequency domain analysis approach based on mathematical convolution of the channel with the digital data. This requires support of new IBIS-AMI I/O modeling and frequency domain channel simulators. The use of S-parameter modeling shows very good results and will continue to help improve the level of accuracy in simulations.

De-embedding DDR4 Interposer and Probe

An ideal scope probe has infinite input impedance. However, probes available today do present additional loading on the circuit under test. Understanding the effects of probe loading over frequency is an important part of making good measurements. A schematic for a typical high-impedance probe is shown in Figure 15. At DC, the input impedance is dominated by the 40kΩ and 10kΩ resistors, producing a 50kΩ input resistance per side (100kΩ differential). Between 15kHz and 15MHz, the 260pF and 1040pF capacitors in parallel with the large resistors lower the input impedance. Above 15MHz, the 175Ω and 50Ω series resistors take over the input impedance plot, producing an input impedance of 225Ω per side (450Ω differential). Finally, at frequencies above several GHz, parasitic effects begin to reduce the input impedance further. A plot of single-ended input impedance for this probe is shown in Figure 16. High-impedance scope probes have a fundamental tradeoff between input impedance and noise. In the single-digit GHz range, the probe input impedance is largely dominated by the resistors at the tip of the probe. Increasing the tip resistance also increases the attenuation of the signal while the noise remains the same, so the signal-to-noise ratio is reduced.

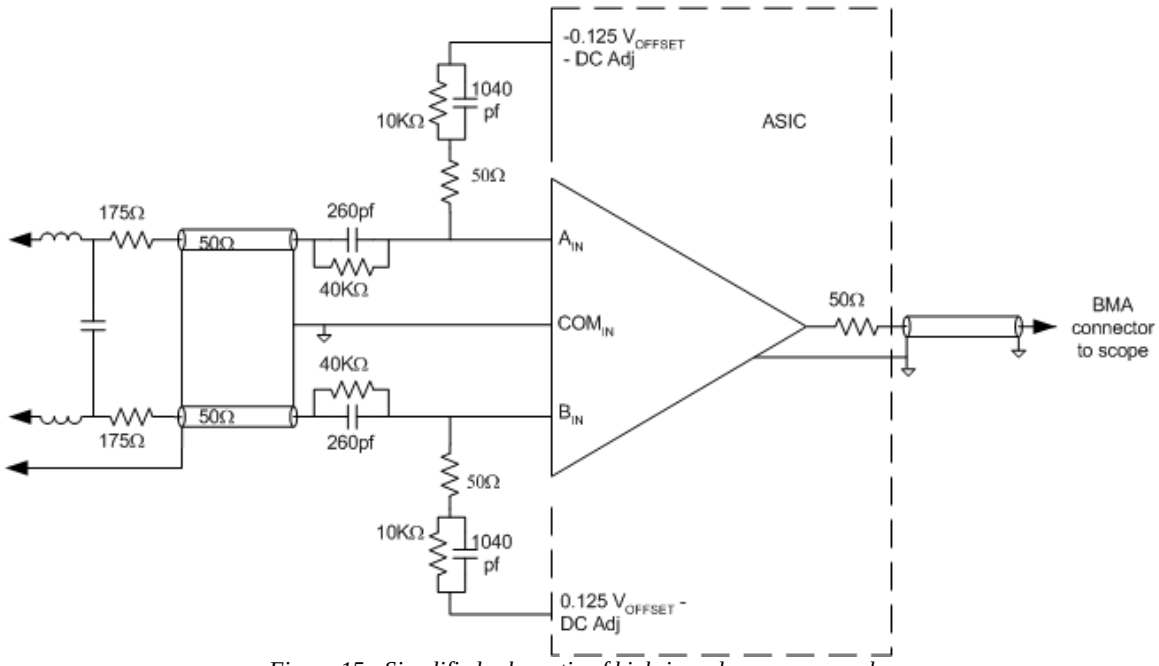

Figure 15 - Simplified schematic of high-impedance scope probe

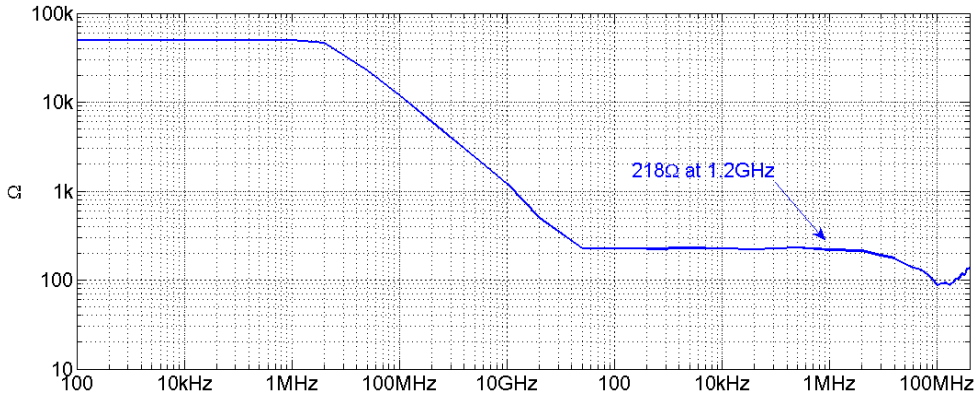

Figure 16- Probe single-ended input impedance

The circuit shown in Figure 17 is a conceptual schematic of a single-ended DDR4 data signal with an interposer and probe attached. The circuit impedance seen by the interposer looking into the channel is a combination of the transmitter source impedance, Z_S, the memory termination impedance, Z_T, and the properties of the transmission line between the controller and the memory. For the nominal DC values shown in the schematic, this works out to 26.7Ω. Typically, parasitic pad and package capacitance will lower this impedance as frequency increases. Good signal integrity requires that the tap resistor plus probe input impedance should be large compared to the impedance of the DUT. From the plot of single-ended input impedance of a probe shown in Figure 16, the input impedance is 218Ω at the fundamental frequency of 1.2GHz. The addition of this non-infinite shunt impedance has the effect of attenuating the signal seen by the receiver by about 1dB. This is typically not enough loading to disrupt proper circuit operation, but is large enough to noticeably alter the waveform displayed on the scope. The insertion loss associated with probe loading is automatically compensated in the probe

with an assumption of 25Ω source impedance. Deviation from 25Ω source impedance, either at DC or over frequency, requires further de-embedding as described below.

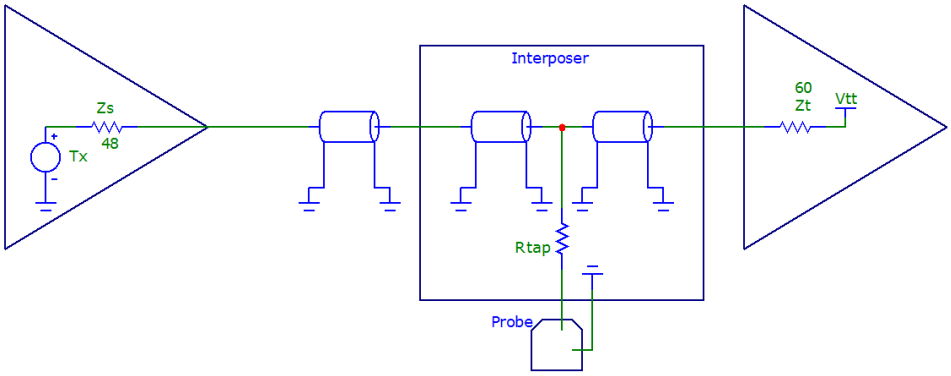

Figure 17- Single-ended DDR4 schematic with interposer and probe

The insertion loss of the interposer is another source of DUT loading. The interposer S-parameters reveal the insertion loss of the interposer assuming a 50Ω load on Port 3 (the probe tap port). Since the input impedance of the probe is significantly larger than 50Ω, a more representative view of the actual insertion loss requires that the S-parameters of the probe to be cascaded with Port 3 of the interposer. This system insertion loss is shown in Figure 18. The total insertion loss of 1.05dB at 1.2GHz is comprised of about 0.95dB from the probe loading effect; the gap between the probe input impedance insertion loss and total insertion loss (<0.1dB @ 1.2GHz) can be attributed to the insertion loss of the interposer.

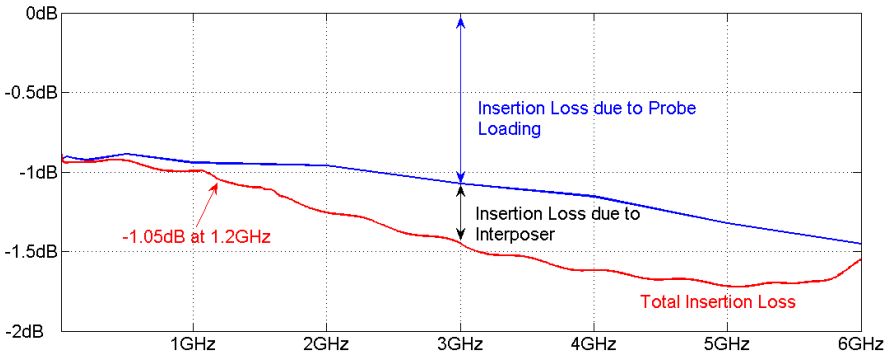

Figure 18- Total Interposer Insertion Loss

For debug, decoding or troubleshooting measurements, the insertion loss introduced by the interposer and probe is acceptable. For compliance or margin testing, these effects become more important and require de-embedding to provide a view of what the unloaded waveforms look without probing. De-embedding can remove any bandwidth-limiting or distortion effects of the interposer and probe. Another advantage of de-embedding is that it allows viewing waveforms at points that are not accessible to probing such as at the memory ODT. De-embedding can be performed by post-

processing oscilloscope waveforms; however, it is often more convenient to de-embed the data in real-time while the measurements are made on the oscilloscope. The de-embedding algorithm must take into account the Tx and Rx impedances and how they vary over frequency. In order to remove reflection effects caused by probe loading, the parameters of the transmission line must also be known. Figure 19 shows a model chain used inside an oscilloscope to de-embed measurements. This model allows for transmitter, receiver and transmission properties to be captured. Interposer and probe S-parameters are also used to account for loading effects. After all model parameters are gathered, a FIR filter is generated that is convolved with the measured waveform and updated real-time on the scope display.

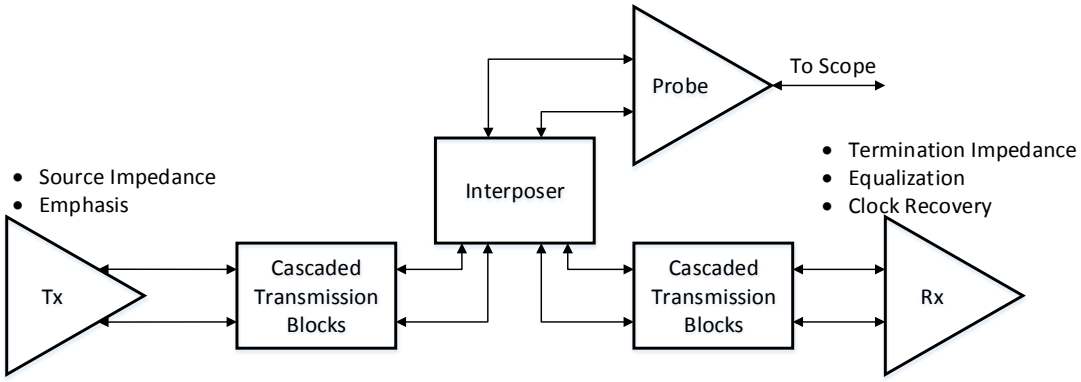

Figure 19- De-embedding Model Block Diagram

A filter generated to de-embed the interposer and probe from a DQ0 measurement is shown in Figure 20. There are only minor adjustments to frequencies at the fundamental (1.2GHz) and below which primarily serve to correct for the DDR4 impedances and flatten the response. At the third harmonic (3.6GHz), about 2dB of correction is applied.

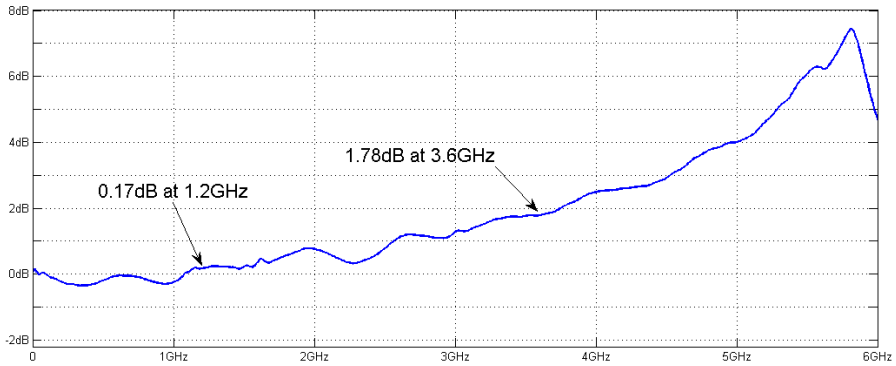

Figure 20 - DQ0 De-embedding Filter

Figure 21 shows a scope screen-shot containing the DQ0 signal that was measured above. The de-embedded signal has smaller amplitude to correct for slightly larger source impedance than the nominal 25Ω. Also, the third harmonic is more evident in the increased distortion of the de-embedded waveform, correcting for the larger insertion loss at 3.6Ghz. As frequencies increase, de-embedding will become a critical piece of the measurement process.

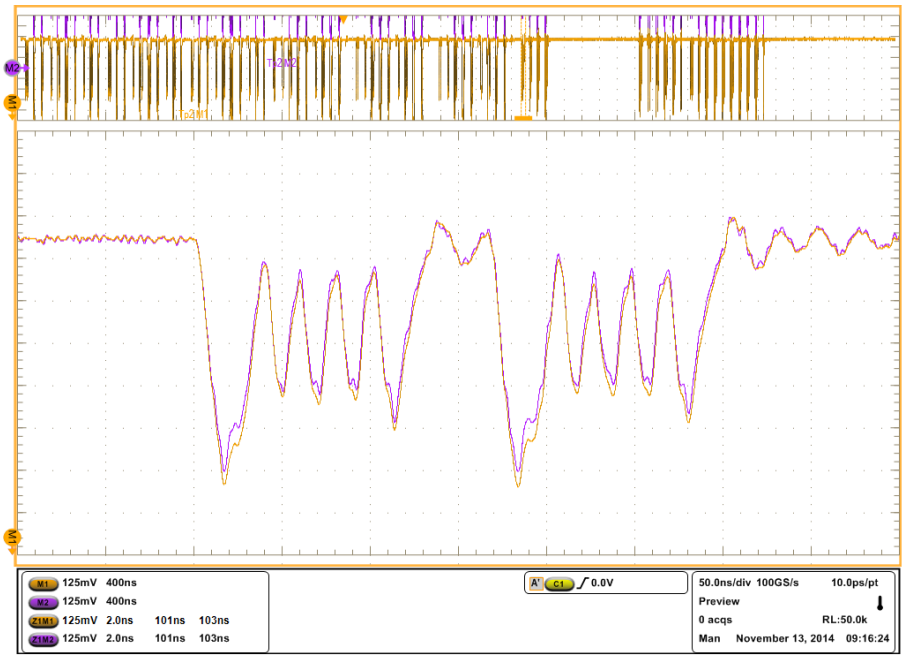

Figure 21- DQ0 signal with interposer/probe (orange) and de-embedded (purple)

Interposer Characterization

There are a number of factors complicating the measurement of interposer S-parameters. Interposers are small interconnects that do not easily connect to measurement equipment. Various methods including striplines launched into the interposer vias and direct large pitch probing are necessary to connect the interposer to the VNA. A typical SOLT or SOLR calibration established reference planes at the ends of the VNA cable and these reference planes need to be translated to the interposer. The launch transitions into the interposer vias present real signal integrity challenges.

Ideally, each signal pin (or differential) pair would be surrounded by ground connections spaced to match the expected termination impedance. DDR4 also has an additional constraint on the number of pins available. As a result, the DDR4 ballout, as shown in Figure 22, is a tradeoff between all concerns. The DQ5 signal located at grid D8 is surrounded by six high-frequency grounds (at grids C7, C8, C9, D9, E9 and E8) and two signal nets (at grids D7 and E7). At high frequencies, the return current will be spread principally across the six high-frequency grounds. However, the RASn signal (located at grid H8) has only two adjacent high-frequency grounds (VSS and VDD). Terminating the adjacent signals in a manner representative of the expected application was found to be necessary for the most accurate results.

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c[3]				DM_n, DBI_n TDQS_t[2], (NC)[1]	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4 (NC)[1]	DQ2				DQ3	DQ5 (NC)[1]	VSSQ	D
E	VSS	VDDQ	DQ6 (NC)[1]				DQ7 (NC)[1]	VDDQ	VSS	E
F	VDD	(C2)[5] ODT1[6]	ODT				CK_t	CK_c	VDD	F
G	VSS	(C0)[5] CKE1[6]	CKE				CS_n	(C1)[5] (CS1_n)[6]	TEN (NC)[7]	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				A17 (NC)[4]	A13	VDD	N

Figure 22- DDR4 SDRAM X4/8 Ballout

Two approaches were used to physically measure the interposer S-parameters for this project. The first approach connected to the three ports using microwave probes. This technique, known as the "flying probe" method, had the advantage of being relatively quick and straight-forward. A drawback of the flying probe measurement method is that the return path for each port is restricted to one adjacent ground or power connection. At higher frequencies, the return path effects become significant.

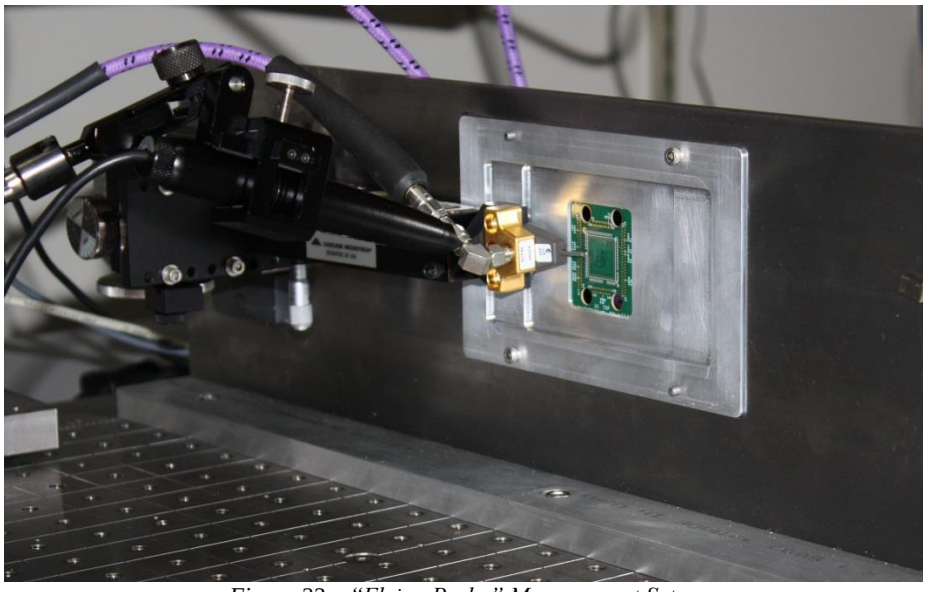

Figure 23 – "Flying Probe" Measurement Setup

Although easy to conceptualize, the flying probe method has some practical obstacles to overcome. Figure 23 shows a picture of a flying probe interposer measurement setup. In order to measure ports on both the top and bottom, a fixture was used to hold the interposer under test vertically, allowing access to both sides. Once the practical issues of mechanically probing the various interposer ports are resolved, only a 2-tier VNA

calibration is required. The calibration is further aided by software from the microwave probe vendors that interfaces with the VNA to measure the calibration standards and update the calibration factors for the measurement. The insertion-loss and return-loss correlation plots for the flying probe method and a simulation with equivalent ports is shown in Figures 24 and 25. The insertion loss measurements agreed to the simulation to within a few tenths of a dB up to 6GHz; the return loss measurements were within about 2dB over the same frequency range. These results demonstrate that the simulation has captured relevant interposer features.

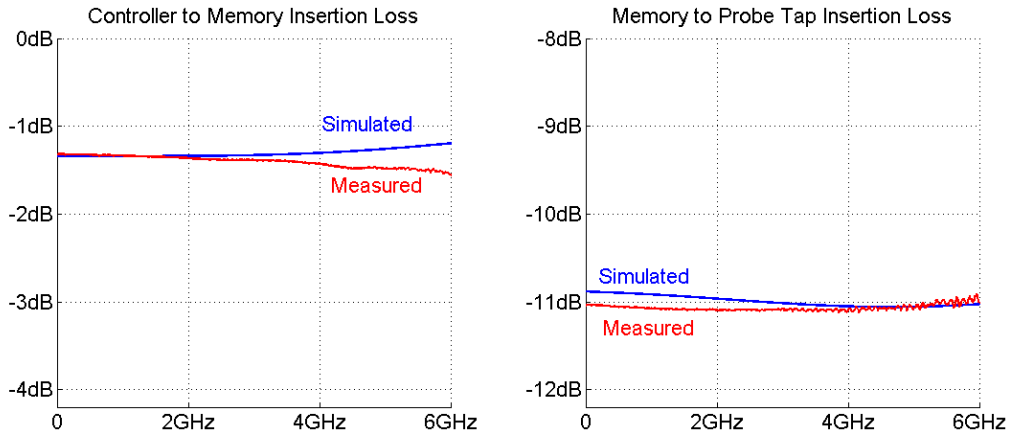

Figure 24- Flying Probe Insertion Loss Correlation

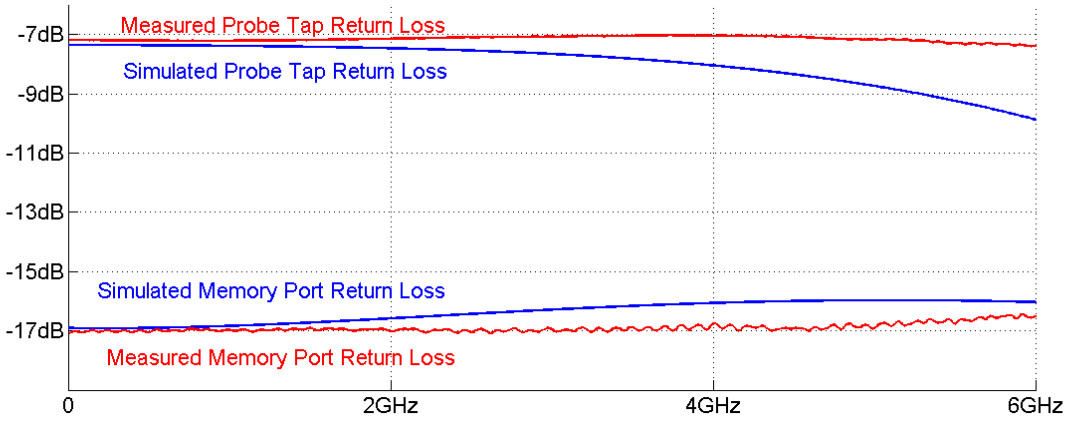

Figure 25- Flying Probe Return Loss Correlation

The flying probe measurement is a valuable way to take a good measurement of an interposer. However, as mentioned above, constraining the return current to only one through via is not the most realistic condition. In order to measure the interposer S-parameters with connections as close to the application as possible, we partnered with WildRiver Technologies to develop an interposer test platform (shown in Figure 26) which ties all power and ground connections in the interposer together as a return path. This measurement method will be called the "Mounted Measurement" method. The test fixture consists of a daughter card specific to the interposer under test and a motherboard that includes 2.92mm connector breakouts of measured nets on the interposer. The

daughter card connects directly to the controller-side of the interposer and the castellations[4] for the probe taps. It is connected to the interposer with a pariposer[5] fabric to provide a repeatable connection with excellent signal integrity.

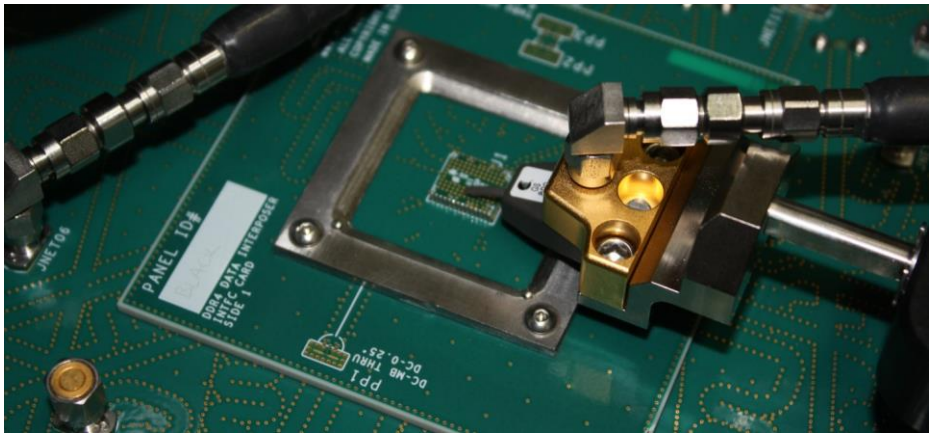

Figure 26- Interposer Characterization Platform

The daughter card and motherboard each contain calibration structures which allow for material characterization and de-embedding measurements to be made. An additional calibration daughter card (shown in Figure 27) provides a mechanism for further calibration measurements. The memory connection is probed with a microwave probe.

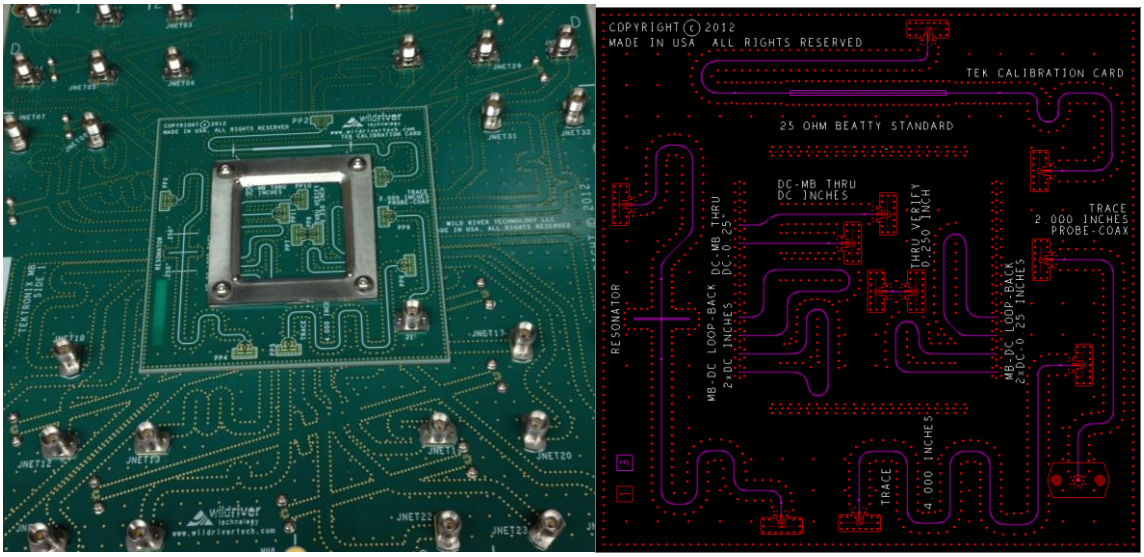

Figure 27- Motherboard with Calibration Card Replacing Interposer DUT (left) and Calibration Card Layout (right)

The measurement process for the interposer-mounted fixture requires a four-tier calibration process. The first and second tiers are the VNA cal to 2.92mm connectors and the addition of the microwave probe calibration. The third calibration step involves measuring on-board test structures that consist of a loopback on the daughter card that has twice the path length of the motherboard connector to interposer net. By designing

[4] http://www.viasystems.com/documents/technology/application-note-castellated-holes.pdf
[5] http://www.connect2it.com/pdfs/elastomer.pdf

the calibration card to have loopbacks on the same nets as are used to measure the interposer, the specific traces used in the measurement can be characterized. The 2X through measurement is then split into two parts. An important part of the fixture splitting is evaluating the S-parameters in the time domain to make sure that all reflections and delays are consistent with the geometry of the measured device. When de-embedding relatively long traces (compared to the interposer length), small errors in the splitting algorithm are readily apparent as reflection artifacts that correspond to the de-embedded trace delay. The fourth calibration is to de-embed the split 2-port S-parameters produced by step 3.

Figures 28 and 29 compare the flying probe measurements and the mounted measurements. The flying probe measurement constrains all return current to flow through only one surrounding via. The mounted measurement has multiple return paths, similar to the conditions when the interposer is installed in a circuit. The electric fields and therefore losses are different between these two cases. The two insertion loss plots show significant divergence above 1GHz, indicating that some of the energy is either coupled into unmeasured nets or absorbed by the interposer. Further investigation is necessary to better understand the interposer performance in this configuration.

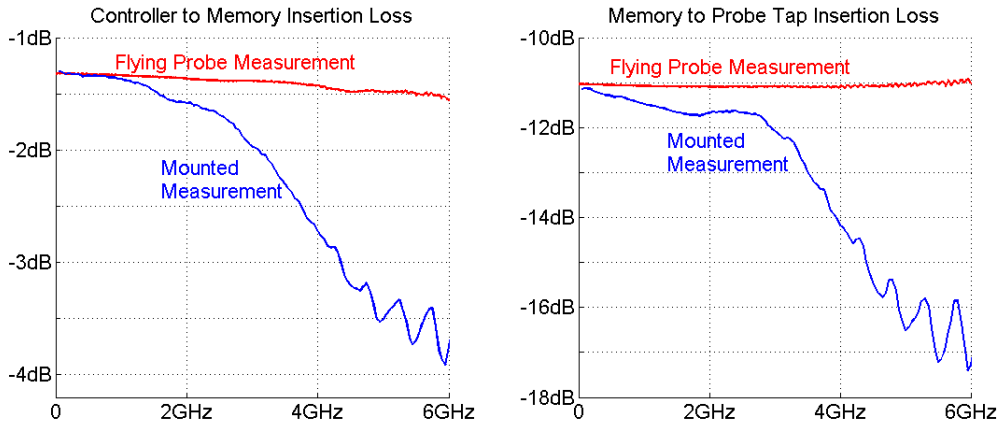

Figure 28- Insertion Loss Measurements for Flying Probe and Mounted Measurement Methods

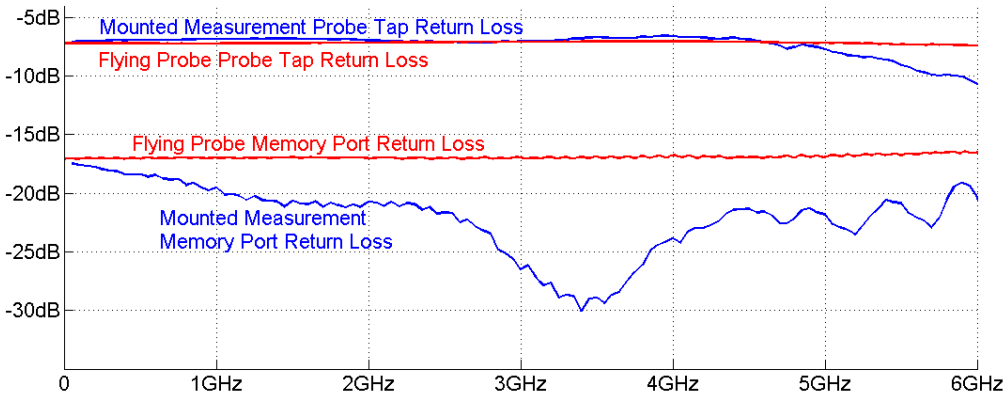

Figure 29- Return Loss Measurements for Flying Probe and Mounted Measurement Methods

Conclusion

This paper presents the challenges of taking measurements in tightly confined space for high-speed DDR signals and the benefits that can be realized using the DDR interposer approach. S-parameter metrics and modeling are introduced to evaluate the performance of the interposer design as well as extending the simulation accuracy. The measurement and correlation sections provide a performance benchmark and hardware validation.

The use of 3 and 6 Port S-parameter modeling of the DDR interposer help provides a more intuitive understanding of the electrical interconnects. As the industry continues to push toward smaller form factors for mobile products with greater speed and density, new advancement in measurement techniques such as the flying probe and network de-embedding will continue to play a crucial role. The detrimental effects of the parasitics at high frequency can no longer be ignored. As of this writing, further work is in progress to provide solutions for low power SoC and fine pitch mobile memories such as LPDDR4 with 0.4mm BGA pitch and 4266MT/s.